SECTION 9

OPTIONS — THEORY OF OPERATION

9.0 GENERAL

This section addresses the two external Data Entry Systems (2115 and 2116) and the two Recorder Boards (6808 and 6666) which are options available for use with the 115 Fetal Monitor.

9.1 MODEL 2115 DATA ENTRY SYSTEM

The Model 2115 Data Entry System is an option that plugs into the back (J103) of the Model 115 Fetal Monitor. This option is a 16 key membrane-type keypad designed to print messages and data on the strip chart of the Model 115 Fetal Monitor. The messages and data are displayed on a 16-character LCD on the front of the keypad before being printed.

Predetermined Messages

The 13 function keys are capable of printing the following predetermined messages:

- Blood Pressure
- Vaginal Exam
- Position Change
- Temperature
- Rupture of Membrane (ROM)
- Oxytocin
- Pulse
- pH
- IV
- Respiration
- Fetal Movement (FM)
- Oxygen
- Medication

In addition, an event mark can also be printed.

Model 2115 Subassemblies

The Model 2115 Data Entry System consists of the following five subassemblies:

- Processor Board (5809)
- Keypad Composite (5840A)
- Auxiliary Board (5983A)
- LCD Display Unit (5958A)
- Main Cable Assembly (5959A)

Processor Description

All data and control operations are performed by the hardware and firmware (ROM) located on the 5809 Processor Board. This includes communications between the keypad and Model 115 Monitor and the keypad and the LCD display. In addition, the processor board also contains and executes the following test routines.

After power-up, the system processor (U1) initializes the LCD display by:

1. Setting the display mode.
2. Loading the special display characters into the display RAM.
3. Clearing the display.

Power-Up Test Routine

After completing these operations, the processor begins a power-up test routine. This routine places the "WAIT" message on the display. After displaying this message, the processor samples the BUSY line (pin 6 of U1) from the Model 115. If this line is a logic low, the Data Entry System remains in a loop waiting for this line to go high.

After the BUSY line is sensed high, the following sequence occurs:

1. The routine tests its system RAM and the link to the Model 115 Fetal Monitor. The link test is initiated by sending a test message (00H) to the 115.
2. The 2115 then waits for the 115 to acknowledge the message. The 115 accomplishes this by lowering the IBF line (pins 4 and 5 of U2).
3. After detecting the acknowledge, the 2115 waits approximately 60 μs to allow the Model 115 time to process the test message.
4. The 2115 tests the status of the INVLD line (pin 39 of U1).

A logic low on this line indicates that the message sent was determined to be incorrect. If this happens, the 2115 displays an "ERROR 3" message and enters a halted state. To clear this error, the Model 2115 must be unplugged from the back of the Model 115 and reinserted into its socket. (NOTE: "ERROR 1" indicates the failure of the 115 to accept data during the mainline routine. "ERROR 2" indicates the failure of the *U1 RAM which requires its replacement.*) If the INVLD line does not go low following the 60 μs delay, the Data Entry System assumes the correct message was received and responds by issuing the END OF STRING (EOS) message (10H). After sending the EOS message the 2115 exits the test routine. (All messages sent to the 115 must be terminated with the EOS byte to indicate that the transfer is complete.)

Functional Description

Upon successful exit from the test routine, the Model 2115 displays a "READY" message to the user to indicate the system is operational. Once in the "READY" state the system processor begins the scan portion of the software. During this section of the program, the 2115 scans the keyboard looking for a keypress. If no keypress is detected, the routine tests the status of the BUSY line. If the BUSY line is low, the BUSY routine is called. In the BUSY routine, the processor monitors the status of both the [Mark Enter] key and the BUSY line while displaying the "WAIT" message. During the BUSY routine the Data Entry System is capable of sending only event marks to the 115 (the event marks are printed only if the 115 recorder is on). As long as the BUSY line remains low the 2115 remains in the BUSY state. When the BUSY line is brought high, the BUSY routine is exited and the "READY" display appears.

9.2 MODEL 2116 DATA ENTRY SYSTEM

The Model 2116 Data Entry System is designed to print messages and data on the strip chart of the Model 115 Fetal Monitor. The keyboard consists of 53 keys by which the user can employ the FREE TEXT MODE for entering comprehensive information or the FIXED TEXT MODE for easy entry of commonly used medical terms, patient parameters, medical procedures, and drug-related information. All data appears on a 40-character LCD at the top of the keyboard for review prior to entry or printing.

Model 2116 Subassemblies

The Model 2116 Data Entry System consists of the following four subassemblies:

- Processor Board (6180A)
- Keyboard Composite (6928AA)
- LCD Display Unit (7064A)
- Main Cable Assembly (7069A)

Processor Description

The 6180 PCB contains the circuitry required to control the functions of the 2116. It is an 8749H processor based system. The 8749H is a single chip containing a processor, ROM, RAM, and I/O ports within a 40-pin DIP. This processor is responsible for the following three major functions:

1. Scanning the 53 microkey keyboard for any key closures.
2. Communicating with the 40-character LCD display.
3. Communicating with the Model 115 Fetal Monitor.

Three additional chips support the 8749H in its tasks: the 74LS157 quad dual-input multiplexor expands the number of I/O ports available to the 8749; a 74LS138 decoder serves as the driver for scanning the keyboard; and a 74LS151 8-input multiplexor senses which key is depressed. In addition to these chips a 74LS05 hex inverter package is used to provide inverters in two places: U1, an ICL7660 voltage converter provides the −5 V necessary to bias the LCD display and U7 provides the 120 VAC needed to drive the LCD backlight.

Functional Description

The RESET signal on pin 3 of J3 is an active high signal coming from a port chip on the recorder PCB of the 115. By inverting this line with U2 (pins 12, 13) an active low reset signal is provided to the RESET/ input of the 8749H. In addition to the reset signal from the 115, the 8749H uses a 1 μF capacitor (C7) to provide a power-up reset signal.

After a RESET has occurred, the 2116 begins its power up sequence by setting the display mode for the LCD, loading the special characters into the display, and clearing the display.

Once these operations have been completed, the 8749H (U4) places a BUSY message in the LCD and begins its power up tests. It begins by testing the BUSY/ line from the 115 (pin 4 of J3) through multiplexor U3 (pin 6). If this line is active the processor waits in a loop for the line to go inactive. Once the transition occurs, the processor tests the link between the 2116 Data Entry System and the Model 115 Monitor as follows.

1. A 5 is placed on the data lines to the 115 (U4, pins 21, 22, 23, and 24 or J3 pins 9, 10, 11, and 12).
2. The nibble is strobed into the 115 by toggling the STB/line (U4 pin 38 or J3 pin 7).
3. The keyboard waits for the recorder to acknowledge the byte by lowering the IBF line (J3 pin 6 or U3 pin 3).
4. After the recorder has acknowleged the byte the ERROR/ line is checked to ensure that the byte was received correctly (J3 pin 5 or U3 pin 3).
5. If no error is detected, steps 1 through 4 are repeated with the following sequence: AH, 1H, 0H.

NOTE: All byte transmissions to the monitor are done by transmitting the byte at two nibbles: high nibble first, then low nibble.

6. If no errors occur during the link test the WAIT message is removed from the display and a LINK OK message appears for approximately 2 seconds. After the 2 second delay, this message is removed and a cursor appears at the left margin of the display.
7. If an error is dectected, the WAIT message is replaced by a LINK ERROR message and the keyboard is placed into a tight loop preventing any further functioning. Once the power-up test has successfully been completed the display shows the cursor at the left margin and the keyboard is ready to process key depressions. The process scans the keyboard by placing a scan code (0 to 7) on the address pins of U5 (pins 1, 2, and 3). This code is decoded by U5 to produce a logic 0 on one of the 8 keyboard scan lines (U5 pins 7, and 9-15). Diodes D1 - D8 are used to prevent one output logic 0 from affecting the other outputs if multiple keys happen to be depressed. Once the scan line has been selected, depressed keys are sensed by sequencing through the 8 return lines using multiplexor U6. By addressing U6 with a code on pins 9, 10, and 11, the state of the keyboard return lines can be sensed on pin 5 of U6. This scanning process is repeated until all lines have been scanned. If a key is detected while scanning, the state of the shift keys is also checked by reading the state of the SHIFT/ line (pin 13 of U3). The combination of the depressed key and the state of the SHIFT/line provides the unique code used by the processor to determine the appropriate action. After a message has been built by a series of key depressions, the ENTER key is used to send the message to the monitor. Once this key is depressed, the message is sent in nibble form to the 115 and the ERROR/ line monitored to ensure the message is sent correctly. If an error is detected, the entire message is resent. If three failures of a single message are detected, a MESSAGE ERROR is displayed and the message aborted.

Throughout all scanning, three additional lines are monitored. These are the BUSY/line from the 115, the MARK IN/line from the keyboard, and the TEST signal from pushbutton SW1.

If the BUSY/ line is detected low, the keyboard displays the WAIT message in the display and stops all keyboard scanning except for detection of the MARK IN/ line. This line goes low whenever the 115 cannot accept any more messages either because all printing lines are used, or the recorder has been turned off.

The MARK IN/ (pin 14 of U3) goes low when the user depresses the MARK key on the keyboard. When this happens, the display is cleared and an EVENT MARKER message is displayed for 2 seconds. Also, the MARK/line to the 115 (pin 8 of J3) is lowered for those 2 seconds. After the two seconds has elapsed, any message displayed prior to the MARK being depressed is restored.

The Test switch is used to activate the internal tests of the keyboard. When the pushbutton is depressed, the display is cleared and a menu of tests appears in the display. The tests are selected by pressing the number of the desired test. The tests are listed in TABLE 9-1.

Test No.	Description
1	**ROM Test** A checksum is performed on a section of the ROM to ensure its integrity.
2	**RAM Test** A test of all RAM is performed to verify that it is functioning properly.
3	**Display Test** A pattern of characters is displayed providing verification that all dots in the display are working and all data lines to the display are functioning properly.
4	**Link Test** A test pattern similar to the power-up link test is sent to the 115 Fetal Monitor to check the connection.
5	**Exit** This selection terminates the test mode and returns the keyboard to functional mode.

SELF-TESTS — 2116 KEYBOARD
TABLE 9-1

9.3 RECORDER BOARD W/RS-232C OPTION (6808 or 6666)

The Recorder Board (6808 or 6666) contains hardware and firmware to interface the Model 115 Fetal Monitor with an external computer. It also includes an internal self-test capability.

RS-232C Hardware

Principle RS-232C Hardware includes PROM U9, USART U23, RS-232C compatible gates U24, U25, and counters U16 and U18. Additionally, support hardware includes regulators, U30 and U31, 3-state buffer U15, and their associated components.

8251 USART

The heart of the interface is the 8251A Programmable Communication Interface (USART). This device performs the following functions:

1. Converts 8-bit parallel data on the CPU data bus to a serial bit stream (which is conveyed to the TxD port, pin 19) consisting of 8 serial bits (LSB first), one or zero parity bits, 1 start bit, and is programmed by firmware to send 2 stop bits.
2. Converts an 8-bit stream (from the RxD port, pin 3) to 8 parallel data bits which are strobed onto the CPU data bus (requires 1 start bit, a minimum of 1 stop bit and either zero, 1 even parity bit, or 1 odd parity bit) as programmed by SP2, switches 3 and 4.

3. Sets the baud rate as determined by switches 1 through 10 of SP1 (both transmit and receive).
4. Detects framing and overrun errors (and parity errors if parity-error detection is enabled) which causes the CPU to ignore the data.
5. Generates and accepts RS-232C signals used in modem control and similar applications (DTR, RTS, DSR, and CTS).

USART Initialization and Control

Before any data transfer between the CPU and the 8251A can begin, the USART must be initialized in regards to the baud-rate, character length, number of stop bits, and similar parameters. This is accomplished by the CPU through a sequence consisting of a Reset, followed by writes of command words on the "AD" bus; a command write to the USART indicated by C/D1, WR0 (U23, pins 12 and 10, respectively).

Most of the initialization data is fixed in the firmware with the exceptions of parity enable, parity selection, and baud-rate. These parameters are controlled by the appropriate switches which are sampled by the CPU on power-up via U15.

During operation, in addition to transferring patient data from the CPU to the USART (C/D1, RD0), the "AD" bus is also used to convey a status byte to the CPU (C/D1, RD0). One of the bits in this byte indicates the status of the USART transmit buffer. (Before the CPU can write a data byte to the USART, any previous byte must have been sent out serially and the appropriate flag bit set indicating that the buffer is empty). Other bits are flags indicating parity error, overrun error, and framing error.

In the Transmit/Receive Mode, the 115 must also be able to receive serial data from the external computer via the RS-232C Interface. When the USART receive buffer contains a received byte, it drives the RxRDY line high (pin 14, U23).This initiates a RST 5.5 interrupt routine which causes the CPU to service the interrupt (on a priority basis with the RST 7.7 interrupt at top priority) and accept the byte.

RS-232C Logic Interface

Salient features of the RS-232C Specifications (EIA) for interfacing data-processing equipment are as follows:

1. Voltage magnitudes for logic levels must be between 5 and 15 V for a 3000 to 7000-ohm load.
2. Levels are positive for logic 0 and negative for logic 1.
3. Logic transitions must not exceed a slew rate of 30 V/μs.
4. Output devices must be able to withstand a short between any of the interconnecting-cable conductors.

The USART is a TTL device and is not directly compatible with equipment which satisfies the foregoing specifications. Gates U24 and U25 along with regulators U31 and U31 serve as the interface between the TTL levels of the USART and RS-232C devices.

U24 is a type MC1488 line driver with approximately 300 ohms of output resistance. This resistance in combination with the 330-pF capacitor ensures the slew rate is below the 30-V/microsecond tolerance. Regulators U30 and U31 provide the ±12V supplies required by the gates to interface with the RS-232, RS-232C levels. Additionally, the regulators internal output transistors disconnect the gates during power off. This is necessary since a short of all four gate outputs to ± 15 V exceeds the device rating if the Vcc and Vee inputs are connected to a low-impedance during power off. U25, an MC1489 Line Receiver accepts the RS-232C signal levels from the external computer and converts them to TTL levels for the USART.

USART Clocks

There are two clock functions required by the USART:

1. Synchronization with the microprocessor clock for data and command transfer via the data bus. Pin 20 (CLK) of U23 is tied to pin 37 (CLK OUT) of U5, and performs this function (CLK OUT is 1/2 the frequency at pin 1, U5 giving 3.072 MHz).
2. Clock signals to set the baud rate of the transmitted and received data streams. These functions are performed by U2, U16, U17 and U18.

The baud rate is set by the clock signal appearing at the RXC and TXC inputs (pins 25 and 9) of U23. During initialization, these inputs are programmed internally as divide-by-16 counters.

The RXC and TXC clock signals are also derived from 3.072 MHz via the divider chain consisting of U16 and U18. U16 is a divide-by-10 counter which drives the U18 "CPA" clock input at 307.2 kHz.

The output frequency from U18 (which is a dual binary counter) to U23 depends on the baud rate selected by SP1 as follows:

BAUD RATE	OUTPUT FREQUENCY (U18)
9600	153.6 kHz
4800	76.8 kHz
2400	38.4 kHz
1200	19.2 kHz

COUNTER OUTPUT FREQUENCY
TABLE 9-2

The 19.2 kHz signal serves as the clock for the other binary counter in U18. For the 300 baud rate, this signal is divided by 4 to 4.8 kHz. The selected signal is then routed to U23 where the internal divide-by-16 counters produce the correct frequency for the desired baud rate.

300 Baud Detect

Heart rate and UA data are not sent at the 300 baud rate. Selection of the 300 rate is detected by the microprocessor (U5) via the U6 PIA PB1 port (pin 30). This port is driven high if SP1 is in the 300 baud position.